A NEW CHIP INTERCONNECTION TECHNIC FOR ULTRA HIGH-SPEED AND MILLIMETER-WAVE APPLICATIONS

Gerhard Hanke and Wolf-Dieter Nohr

Deutsche Telekom - Technologiezentrum
P.O.Box 10 00 03, 64276 Darmstadt, Germany

Abstract

Nearly lossless and non-reflecting interconnections between semiconductor-chips and transmission lines working up to 50 GHz can be realized in a "Reverse Beam-Lead Technic" as well as low-impedance ground and power supply interconnections. The paper describes the required technology, compares TDR and S-parameter measurements of state-of-the-art technics and the new one, and gives some examples of high-speed circuits.

Introduction

Conventional interconnection technics (wire bonding, beam-lead, flip-chip) show more or less unsatisfactory results at millimeter waves or ultra high-speed applications [1]. To reduce discontinuities and therefore also losses and reflections at the transitions between pads on semiconductor chips and transmission lines on hybrid substrates we developed a new interconnection method which we call "Reverse Beam-Lead Technic" [2]. Furthermore we are also able to realize very low-impedance interconnections to ground and power supplies. Measurements show that this technic is useful up to more than 50 GHz.

Reverse Beam-Lead Technology

The contribution describes a new possibility of inserting and inner lead bonding of semiconductor chips in film circuits. This technology is suited, apart from its generally favourable applicability to the setup of multi-chip modules, especially for the implementation of ultra high-speed circuits. The basic principle of the chip interconnection technology presented is, that the semiconductor chip to be inserted is mounted flush with the film circuit surface into a previously prepared chip-sized substrate opening from the reverse side of the film circuit. Leads as part of the film circuit project into the substrate cutoff and are bonded by means of, for instance, soldering. Adjustment and placement of the chips to the leads are performed individually using a face-down component placement device. The flush chip mounting and the possibility of exact geometrical adaption of the leads to the conducting structure of the semiconductor chips provide a circuit configuration with remarkable low impedance discontinuities and with low electrical attenuation. A description of the photolithographic manufacturing of the lead structure with the contacts as well as of the bonding process is given.

Figure 1 shows an experimental structure of a thinfilm circuit with microstrip lines of different widths (25, 50 and 100 µm). The substrate opening is 1 mm by 1 mm, the substrate thickness is 254 µm. The leads project about 200 µm into the opening. Figure 2 is an electron microscope photo of the three types of leads.

Measurements

To compare the "reverse beam-lead" interconnections with conventional ones TDR (HP 54124A) and S-parameter (HP 8517A) measurements with 50 Ω microstrip lines were done, measurements with 50 Ω coplanar waveguides have, due to connector problems, not yet been finished, but will be presented at the conference.

The structures to be compared are shown in Fig 3. The 1 inch by 1 inch ceramic substrates (Al_2O_3 polished substrates, thickness of substrate 254 µm, linewidth 245 µm, thickness of goldlayers 10 µm, length of line 25.4 mm) were structured with 50 Ω thin film microstrip lines, calculated for 20 GHz. As reference structure we used the regular 50 Ω microstrip line, 3.5mm connectors (K-connectors) and a test fixture from Arguments. To simulate the influence of conventional wire bonded connections between strip line and an inserted semiconductor chip we cut out a part of the substrate symmetrically to the center of the substrate. These cut out "chip dummies" were produced with three different gap-widths (minimal, - depending of the minimal laser beam diameter - 50 µm, and 100 µm) to show the influence of gap widths on reflections. As could be expected the minimal gap width gave the best results, therefore only these cases will be examined in the following.

The cut out chip dummy than is inserted back into the substrate, Fig. 3a. The ground layer was connected by an adhesive mounted ground plate to the substrate ground layer. The interruptions of the micro stripline are bridged by one bond wire each (25 µm diameter gold wire).

Fig. 3c shows the mounting of a cut out chip dummy as done in Fig. 3a, but now connected by using the new reverse beam-

0-7803-3246-6/96/$5.00 © IEEE

lead technic. The 50 Ω microstrip line projects for about 200 µm from both sides into the substrate cut off. These leads were performed as a part of the structured circuit after having cut out the chip dummies as described above. Than the dummies are inserted from the rear side into the cutout and interconnected first to the strip line leads and thereafter to the ground layer by soldering.

Results of time domaine measurements with 50 Ω microstrip lines with the HP Oscilloscope 54120A/54118A are given in Fig. 4. The first big reflection, in about 200 ps distance on the left hand side from the center (which corresponds to the middle of the stripline) is the input coaxial to microstrip line transition, the big reflection about 200 ps at the right is the output transition, which is terminated by a 50 Ω resistor. The range between the two perpendicular time markers at the center corresponds to a range of about 2 mm of the stripline and is approximately in accordance with the dummy length.

Fig. 4a is the TDR response of a regular 50 Ω line, Fig. 4b is the response of an inserted ceramic chip (length 1.8 mm, width 0.8 mm, as shown in Fig. 3a) with one bond wire at both ends (the diameter is 25 µm) and a surrounding gap of minimal width. The reflection factor is r = 17 %, Fig. 4c is the response of a 50 Ω line with two gaps of 100 µm each, which are only in the metal layer, not in the ceramic (compare Fig. 3b). The gaps are bridged by one 25 µm bond wire each. The reflection factor is r = 8 %. Fig. 4d is the same inserted ceramic chip as in Fig. 4b, but interconnected in the new reverse beam-lead technic, as shown in Fig. 4c. The reflection factor is r = 4 %.

Results of frequency domain measurements with the HP 50 GHz S-parameter equipment 8510C/8517A in the frequency range from 50 MHz to 50 GHz are given in Figures 5 and 6.

In Fig. 5 the measurement results were calculated into reflection factors by using the low-pass methode. All negative reflection factors correspond to capacitive parasitic components, all positive factors are due to inductive parasitics. Again Fig. 5a is the regular line and the reflections due to the input and output connector can be seen clearely. Fig. 5b is the chip dummy with wire bonded lines which leads to high inductive reflections due to the bonds and the air gaps between substrate and dummy. Fig 5c is the gapped and bonded line without air gaps in the substrate and Fig 5d is the reverse beam-lead interconnection technic which shows neglectable low reflections which can be further reduced by minimizing the substrate air gap.

Fig. 6 gives the results of S_{21} measurements in the range from 50 MHz to 50 GHz. Fig 6a shows the absolute values of S_{21} for the 25.4 mm long 50 Ω microstrip line, Fig. 6b gives the difference between the S_{21} values of the regular line and the S_{21} values of the wire bonded chip dummy (Fig. 3a), Fig. 6c is the difference between the regular and the microstrip line with two gaps and two wire bonds (Fig 3b), and Fig. 6d is the difference between the S_{21} values of the regular line and the S_{21} values of the reverse beam-lead chip dummy (Fig. 3c).

Circuits

To show the advantages of the new interconnections some high-speed and millimeter wave circuits are under construction and will be presented at the conference: A 20 Gbit/s laser driver, a 30 Gbit/s multiplexer and a 40 GHz power amplifier. Fig. 7 is the layout for the 20 Gbit/s laser driver (fabricated in GaAs-HEMT-technology by Fraunhofer-Institute for Applied Physics, Freiburg, Germany [3]). This circuit still uses chip bypass capacitors, in a next step we will integrate thinfilm feedthrough and coupling capacitors, which will be situated as close to the chip as possible.

Fig. 8 shows the terminal area of the chip, which will be placed into the 1mm by 1mm opening. The high-frequency input and output lines are matched 50 Ω lines and tapered to the widths of chip pads. Grounding layers are connected to the reverse side of the substrate by metallized via-holes and are, like the power supply layers, of low impedance.

Conclusion

The presented "reverse beam-lead technic" is an effective tool for ultra high-speed and millimeter wave applications. The optimal results will, however, be obtained by a more sophisticated metallization layout of high-frequency and high-bitrate chips. The impedance of connecting lines on the substrate should continue on the chip. The chips should be cut very exactly to get a gap free fit between chip and substrate cutoff. We are sure that our technic will be applicable also at frequencies of more than 50 GHz. This technology still includes more advantages than we could describe in this short paper. We are working in many directions and for many different applications. One urgent problem is the including of high frequency capacitors for hybrid integration. Some good solutions were found in the mean time with CVD (for bypass capacitors) and Polyimid technics (for coupling capacitors).

References

[1] G. Hanke: "20 Gbit/s Experimental Transmitter and Receiver for Fiber Communication Systems", Proc. IEEE Global Telecommunications Conference, Houston, TX, November 1993, pp. 1144-1148.

[2] W.D. Nohr and G. Hanke: "Reverse Beam-Lead Interconnections for Ultra High-Speed Multichip Applications", Proc. 5th International Conference and Exhibition on Multichip Modules, Denver, CO, April 1996.

[3] Z.-G. Wang e.a.: "Integrated Laser-Diode Voltage Driver for 20-Gb/s Optical Systems Using 0.3-µm Gate Length Quantum-Well HEMT's" IEEE Journal of Solid-State Circuits, Vol. 28, No. 7, July 1993, pp. 829-834.

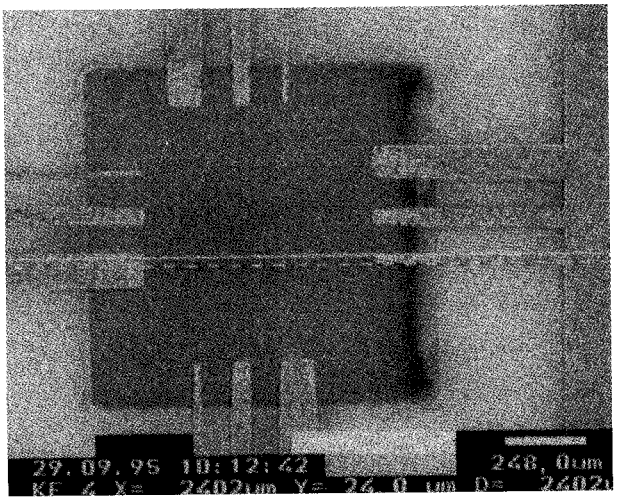


Figure 1 Experimental structure of a thinfilm circuit with micro striplines

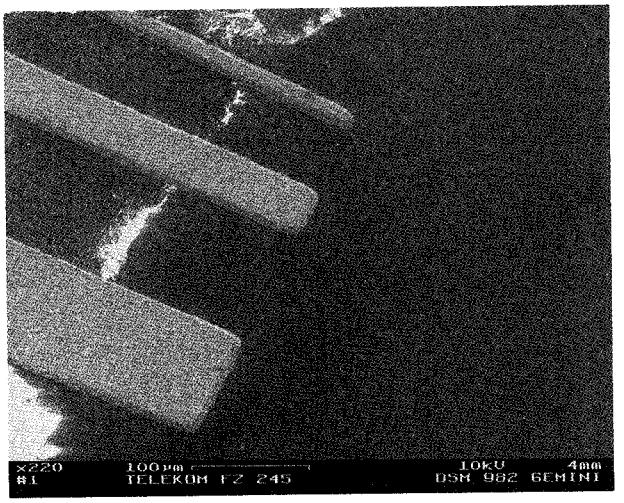


Figure 2 Electron microscope photo of 25, 50, and100 µm leads projecting about 200 µm into the substrate cutoff

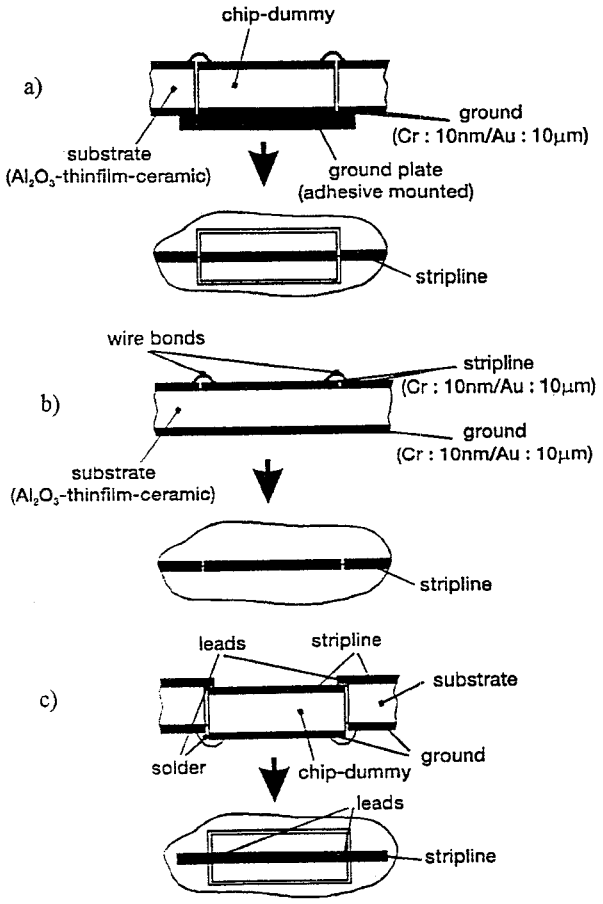
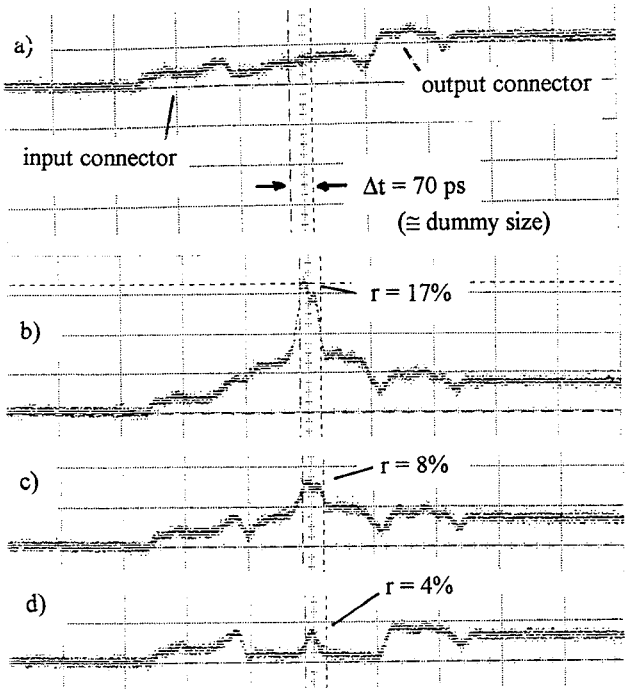


Figure 3 Test configurations for comparing time domain and S-parameter measurements
a) wire-bonded ceramic chip dummy
b) gapped and wire-bonded micro stripline
c) "reverse beam-lead" chip dummy



vert.: 50 mV/div horiz.: 200 ps/div

Figure 4 TDR measurements of 50 Ω micro striplines
a) regular 50 Ω micro stripline
b) wire-bonded ceramic chip dummy
c) gapped and wire-bonded micro stripline
d) "reverse beam-lead" chip dummy

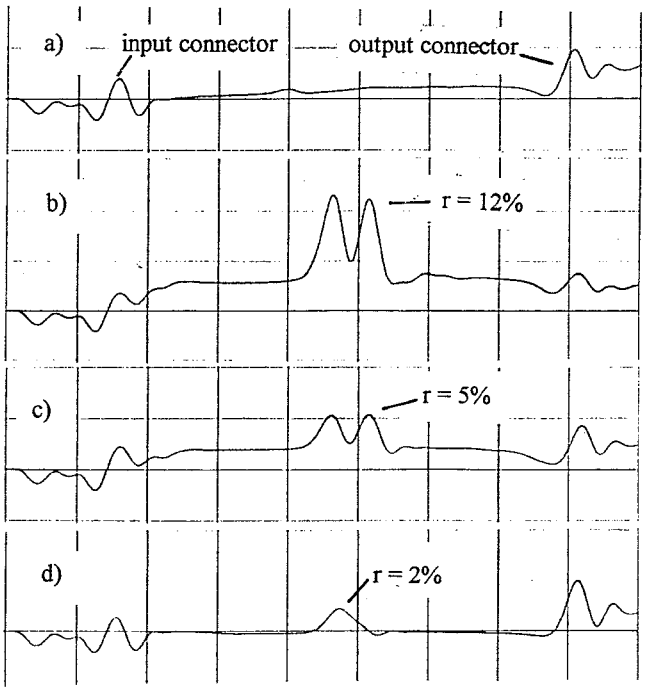


Figure 5 Reflection factors of 50 Ω microstrip lines, calculated (in lowpass mode) from frequency domaine measurements (50 MHz to 50 GHz)
a) regular 50 Ω microstrip line
b) wire bonded ceramic chip dummy
c) gapped and wire bonded microstrip line
d) "reverse beam-leaded" chip dummy

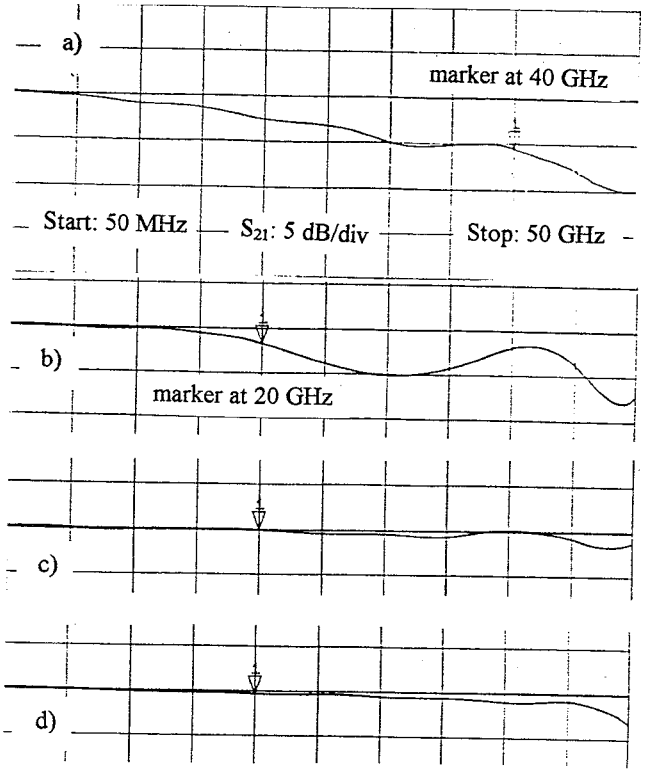


Figure 6 S-parameter measurements of 50 Ω micro striplines (a: absolute values of S_{21}, b-d: differences to a)
a) regular 50 Ω micro stripline
b) ceramic dummy with bond wires
c) micro stripline with gaps and bond wires
d) ceramic dummy with reverse beam-lead interconnections

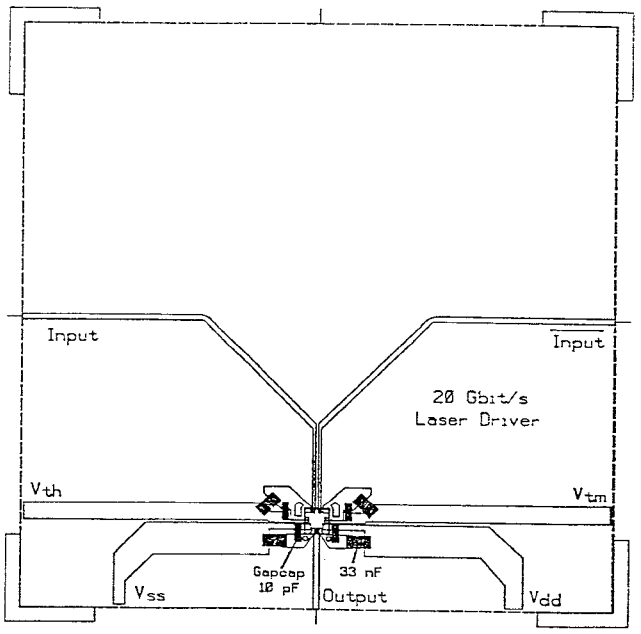


Figure 7 Layout of a 20 Gbit/s laser driver; substrate size is 1 inch by 1 inch

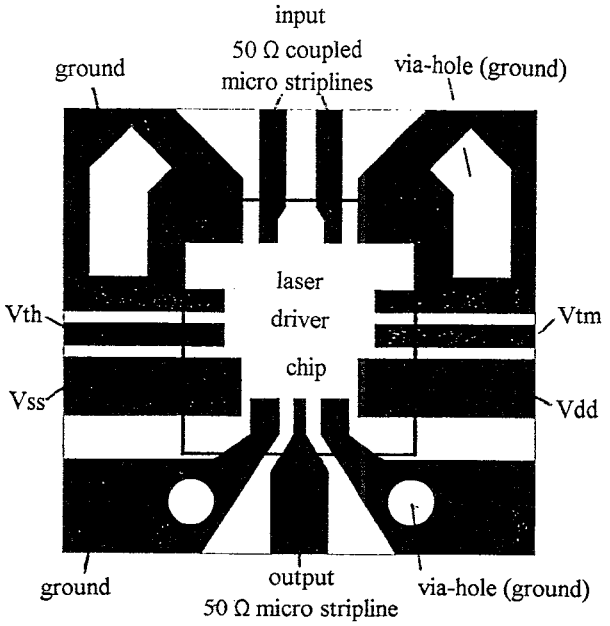


Figure 8 Layout details near the driver chip; chip size is about 1 mm by 1 mm